

Simple Circuits Inc.

# SIMPLE SDR RECEIVER

80 through 17 Meter General Coverage Receiver

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## Simple SDR Receiver

### Introduction:

This document describes the installation, how to operate, and theory of operation of the Simple Circuits Inc. Simple SDR HF radio receiver operating in the 3.5 to 18 MHz range. The receiver architecture is based on software defined radio techniques and incorporates a Cypress PSoC CY8C3866 device that contains both analog and digital circuits, thus decreasing the receiver's component count. This part is far more than just a microcomputer; it also contains software configurable analog and digital peripherals on a single chip. Cypress calls the family a PSoC in reference to it being a programmable embedded system-on-chip. The newest series of parts, which Cypress calls the PSoC 3 family, contains a 67 MHz 8051 class microcomputer, an analog to digital converter fast enough and with enough resolution for an SDR receiver, and other valuable functions that are desirable in a receiver design.

The receiver should be used for casual, conversational listening, not a higher performance receiver for DX use. It was designed to use a minimum number of components, to be physically small, and easy to operate. An LCD display and controls to select the frequency and modes of operations was considered, but the design would have fewer parts and cost less if a personal computer (PC) is used for all user control. Since the PSoC has a USB port, the receiver can connect to the PC with a USB cable and take power from the PC over the USB cable, saving a power jack, and external power source. Control of the receiver is accomplished by the receiver USB port appearing as a standard com port to the PC. The Ham Radio Deluxe (HRD) program works perfectly to control this receiver.

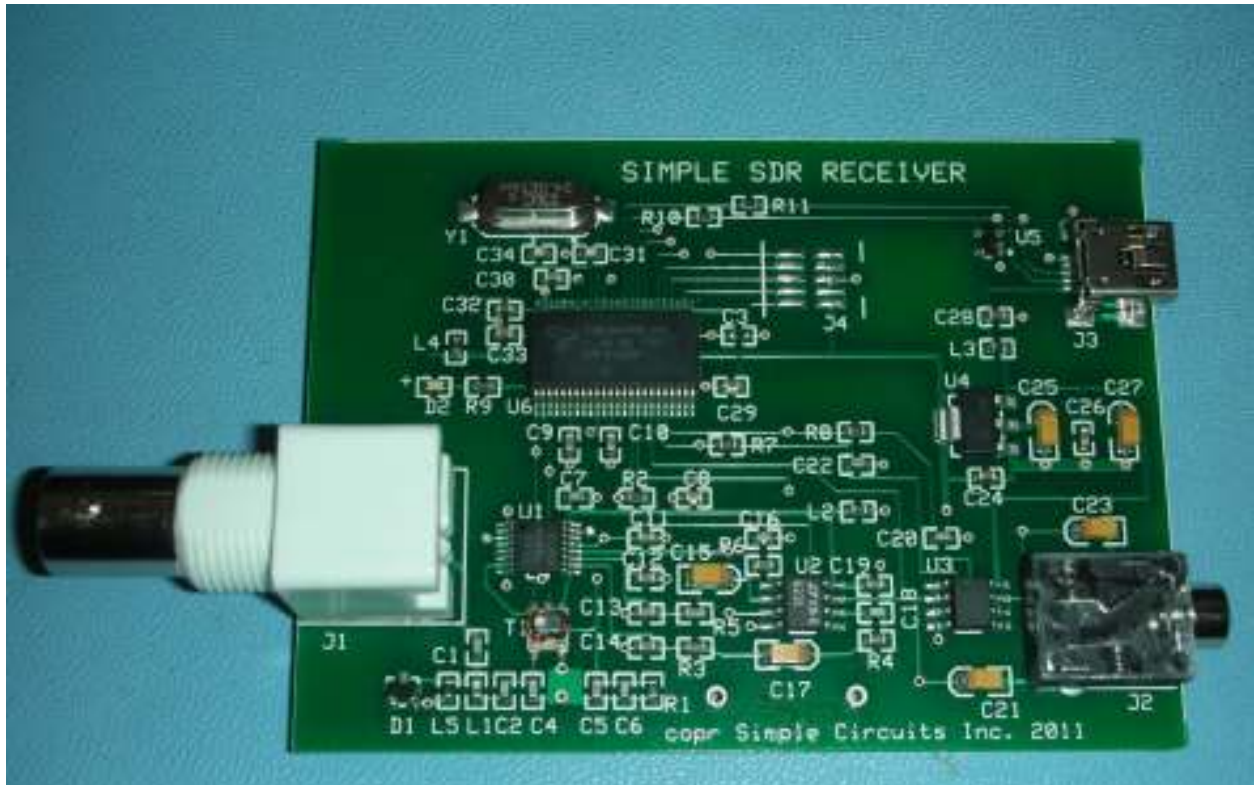


Figure 1: The complete receiver fits on a 3.2 by 2.3 inch printed circuit board.

## **Installation:**

*Before you connect the USB cable*, download the file UARTUSB\_CDC.zip and save it on your computer. Unzip the file, put it in any folder, plug in the USB cable, and the computer will prompt you to either let it search for the driver, or allow you to specify the driver location. You will need to specify the location of where you put the file. The receiver has been tested with XP, Vista, and Windows 7.

Note the com port number that your computer assigned to the receiver. Use that com port number in Ham Radio Deluxe (HRD). In HRD, add a new radio, and select Elecraft K2 as the radio type. The speed setting is not important and can be left as the default value.

## **Operating the Receiver:**

To operate the receiver, perform the following steps:

1. Connect the USB cable between a computer USB port and the receiver's USB connector, J3. Both power and control are provided by this connection. The PSoC has an internal USB full speed port. The receiver firmware implements a virtual serial communication port. When connected to a personal computer, the receiver will look like a serial com device. Using the standard CDC (communication) drivers that are built into Windows, the receiver can communicate with Ham Radio Deluxe. The receiver firmware uses the Elecraft K2 communication protocol.
2. Connect an appropriate antenna to the BNC connector, J1. The antenna should support the desired receive frequency.
3. Connect an audio amplifier or headset to the audio output connector, J2, of the receiver. This connector is a stereo connector, but both channels are feed with the same signal. Therefore, the use of either mono or stereo audio devices are acceptable. The receiver's audio output will directly drive low impedance headsets. The use of good computer speakers that have a built-in amplifier and volume adjustment is ideal. There is no volume control capability in the receiver. Headsets need their own volume adjustments.

The receiver can be continuously tuned from 3.500 MHz to 18.168 MHz (80 through 17 meters).

Using Ham Radio Deluxe to control the radio, the receive frequency, the side band selection, and audio bandwidth can be selected.

There are 4 different receive filter bandwidth selection. Pressing the HRD FILTER button produces a drop down menu with various options. FL1 is a 2.5 KHz low pass filter, FL2 is a 2.0 KHz low pass filter, FL3 is a 1.5 KHz low pass filter, and FL4 is used for CW and RTTY and is a 1.0 KHz band pass filter that is 400 Hz wide (+/- 200 Hz).

The attenuator button, ATT will decrease strong stations audio volume by several dB.

### **Theory of Operation:**

This SDR receiver is built using a quadrature sampling detector, as shown in the block diagram of figure 2. The quadrature sampling detector is nothing more than a set of analog switches that are enabled and disabled in the particular sequence that samples the input signal four times for each cycle of the desired receive frequency. The four samples represent the 0, 90, 180, and 270 degrees of a sine wave. The output of the detector is amplified by a pair of op amp low-pass filters. After the op amps, the remaining signal processing is performed inside the PSoC microcomputer using digital processing techniques. The processing will digitize the baseband signal, remove the undesired sideband from the received signal, limit the bandwidth of the audio, and then convert the digital samples back into an analog audio signal.

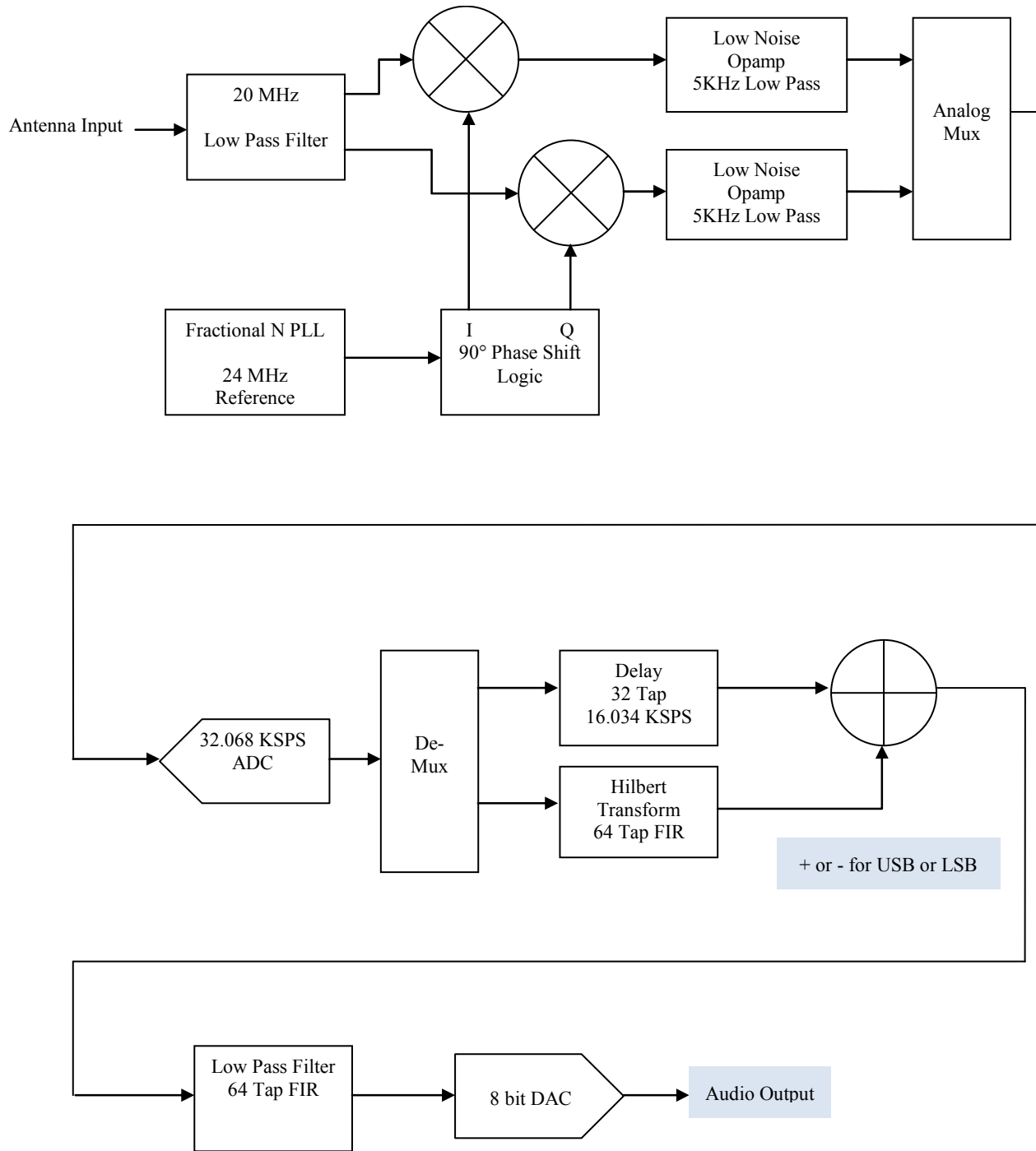


Figure 2: SDR Receiver block diagram.

At the antenna input terminals, an RF low pass filter having a 20 MHz corner frequency suppresses signals above the receiver tuning capability. Figure 3 shows the frequency response for the filter.

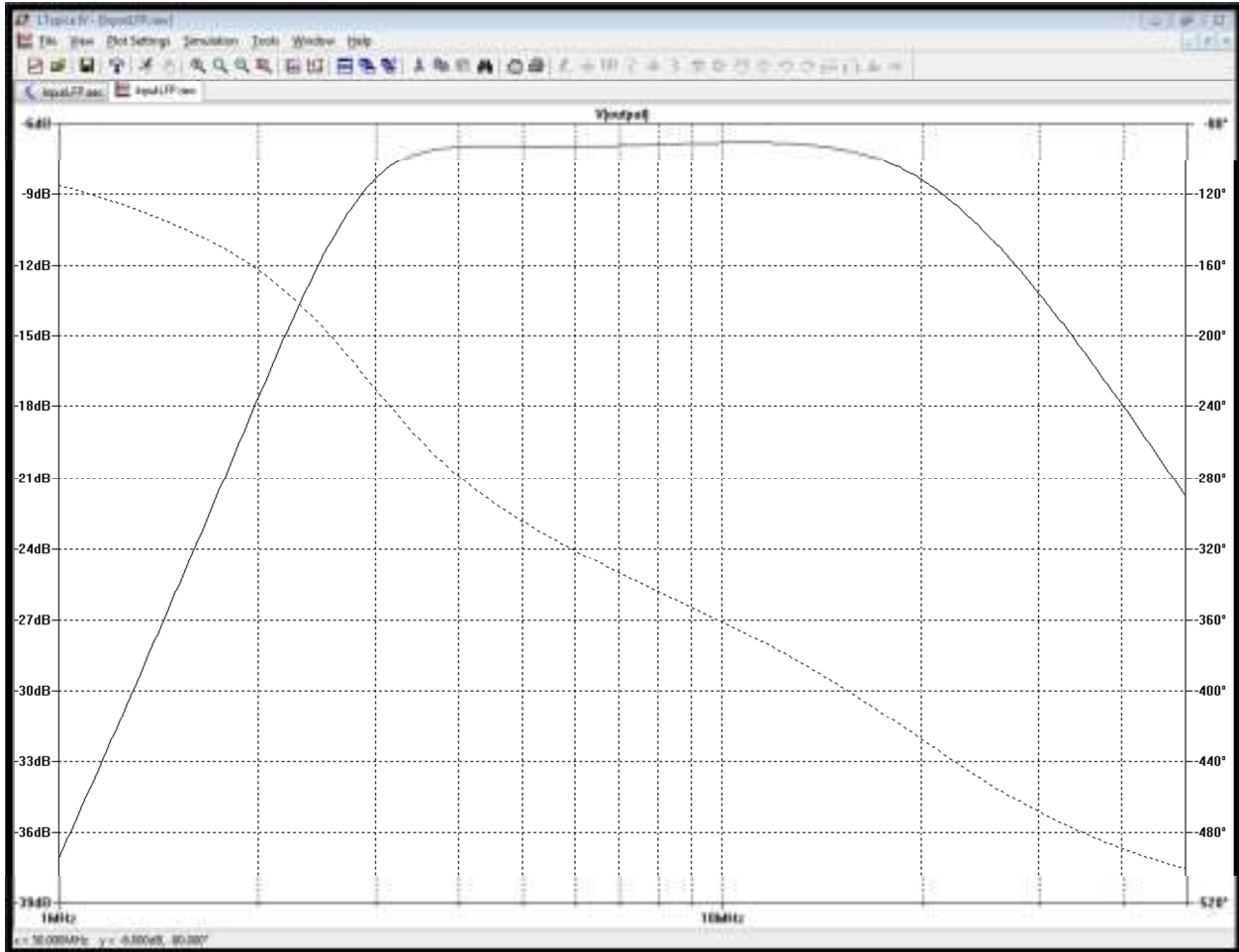


Figure 3: Input RF Filter Response.

Referring to the schematic in figures 6 and 7, U1, a dual 1-of-4 multiplexer/demultiplexer, is used as the sampling detector. This process is similar in functionality as a local mixer, only the control is performed with digital logic switching levels.

The multiplexer is controlled with two square wave clock signals having the same frequency as the desired receive frequency. The clocks only differ in phase, one being delayed by one-fourth of the clock period. This delay represents the 90° phase shift required for an I/Q type detector.

The PSoC has an internal phase lock loop (PLL) circuit that is used to generate higher clock frequencies from a lower speed clock. The receiver makes use of this circuit to generate the sampling detector clock signals. An external 24 MHz crystal is connected to the PSoC that is used as the reference oscillator for the PLL. However, the PSoC PLL only has the ability to generate frequencies that are integer multiples of the clock. An additional logic function was created and added to the programmable digital logic section of the PSoC that modulates the PLL divider registers. This effectively turns the PLL into a fractional N frequency synthesizer. The “fractional” term refers to the capability of dividing the PLL feedback signal by a non-integer number, allowing for a frequency resolution as small as desired. For practical purposes, a 14 bit, sigma delta modulator constructed as a 2<sup>nd</sup> order MASH was written in Verilog. This results in a receiver tuning frequency step size of roughly 50 Hz. When a different frequency is selected, the PSoC firmware computes a set of PLL values that will be within 50 Hz from the display frequency.

An external PLL circuit or discrete digital synthesizer chip (DDS) may generate a cleaner clock, but the advantage of using the internal PLL is obviously component cost savings.

The PLL operates in the 56 to 68 MHz range. A divider function added to the programmable digital logic section of the PSoC divides the PLL oscillator down to the desired receive frequency and shifts the phase appropriately between the two output I/Q clocks.

After the mixing process of the sampling detector, a pair low noise op amps, U2A and U2B, amplify the base band signals. The part was chosen because of its low noise performance and the ability to operate with outputs near the ground and power rails. The inputs to the op amps are typically in the microvolt range. Since the op amp circuit voltage gain is on the order of 40 dB at 1 kHz, the output signals are on the order of a few hundred microvolts to a few millivolts. This circuit includes a first order low-pass filter having a 3 kHz corner frequency. It is important to reduce the frequencies above half of the analog to digital converter sampling rate which is called the Nyquist frequency. Otherwise, images will appear at frequencies near the sampling rate. Figure 4 shows the frequency response of the op amp circuit.



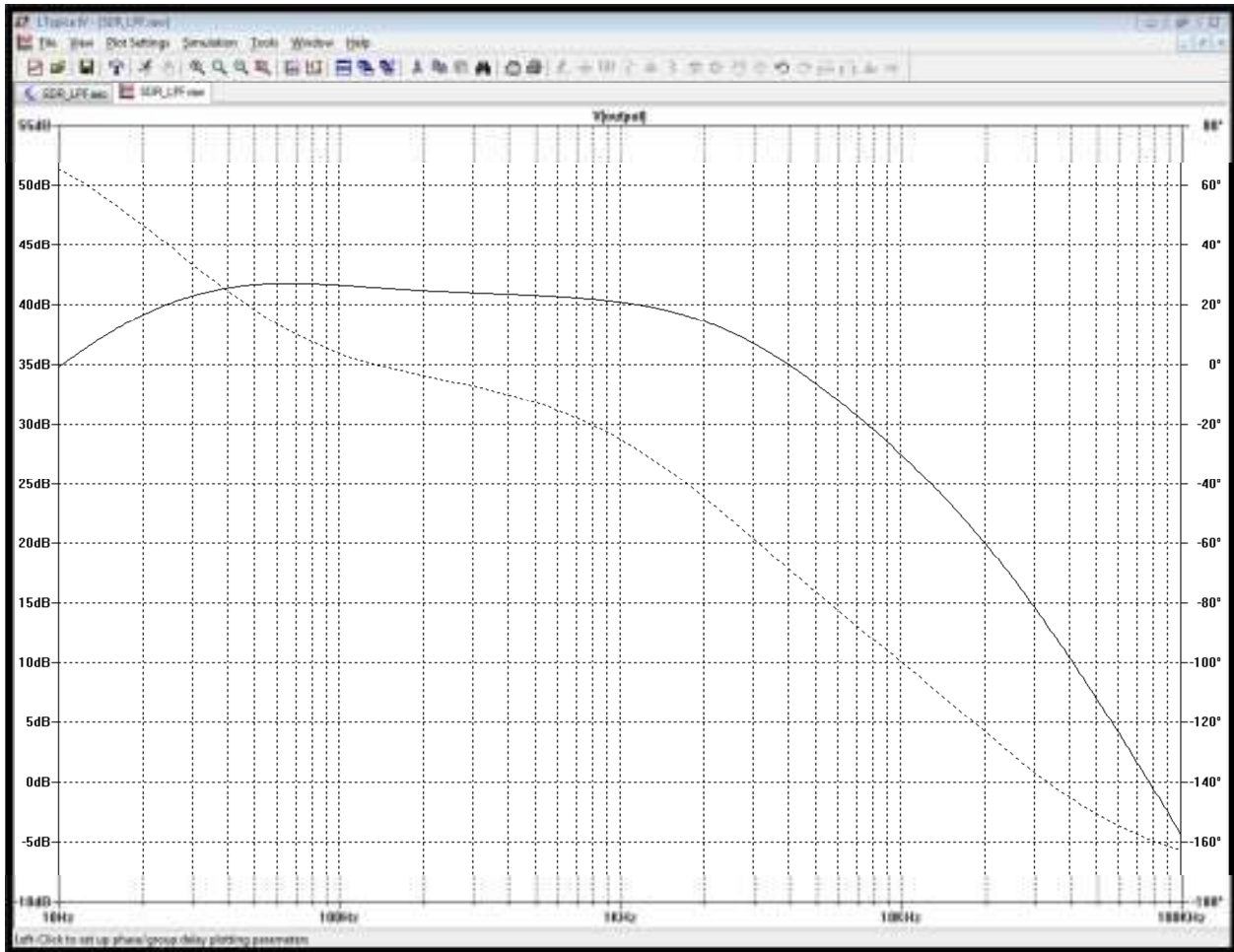


Figure 4: Op amp circuit frequency response.

From this point, all of the signal processing is performed in the digital domain, and, specifically, inside the PSoC, U6.

The PSoC has a single analog to digital converter (ADC). Since there are two base band signals to process, the I and the Q channels, an analog multiplexer function inside the PSoC is used to switch one of the two inputs to the ADC input. It is desirable to have a high sample rate and a high number of bits, but the best tradeoff found was to use the ADC in a 14 bit mode and sampling at 32,068 samples per second. Since a sample from each input channel is necessary, the equivalent sample rate per channel is 16,034 samples per second. Therefore, the Nyquist frequency is almost 8 kHz. The op amp frequency response at 8 kHz is about 10 dB below the desired passband. This is not great, but leaves room for improvement in a future version.

The PSoC 3 family of parts have an interesting internal hardware feature they call a digital filter block, or DFB, and it consists of a 24-bit fixed point, programmable limited scope DSP engine.

This is a dedicated hardware accelerator block that operates independently of the main 8051 processor. It consists of a dedicated multiplier and accumulator that calculates a 24-bit by 24-bit multiply 48-bit accumulates in one system clock cycle. It is optimized to implement a direct form Finite Impulse Response (FIR) filter that approaches a computation rate of one FIR tap for each clock cycle. This block is used as two independent, 64 tap, digital filters.

Alternating outputs from the ADC are loaded into either a 32 sample long delay line or one of the two digital filters. This digital filter uses a set of coefficients that form an all-pass filter having a flat magnitude response, but phase shifts all frequency in its passband by  $90^\circ$ . This is called a Hilbert filter. Suppressing either the upper or lower sideband is accomplished by phase shifting the Q channel baseband data and either subtracting or adding the filter output to the delayed I channel baseband data. The delay is necessary to compensate only for the delays incurred by the processing of the Hilbert filter. The output of the addition is one of the two sidebands.

After the removal of the undesired sideband, the data stream is feed into the other half of the PSoC digital filter block configured as a low-pass filter. This filter has a steep rolloff as shown in the figure 5 for a 2 kHz filter. This is the advantage of processing in the digital domain as compared to a set of analog filters. Steep rolloffs and repeatability of the filter performance over wide temperature ranges and from part to part variations are the reasons to use digital processing.

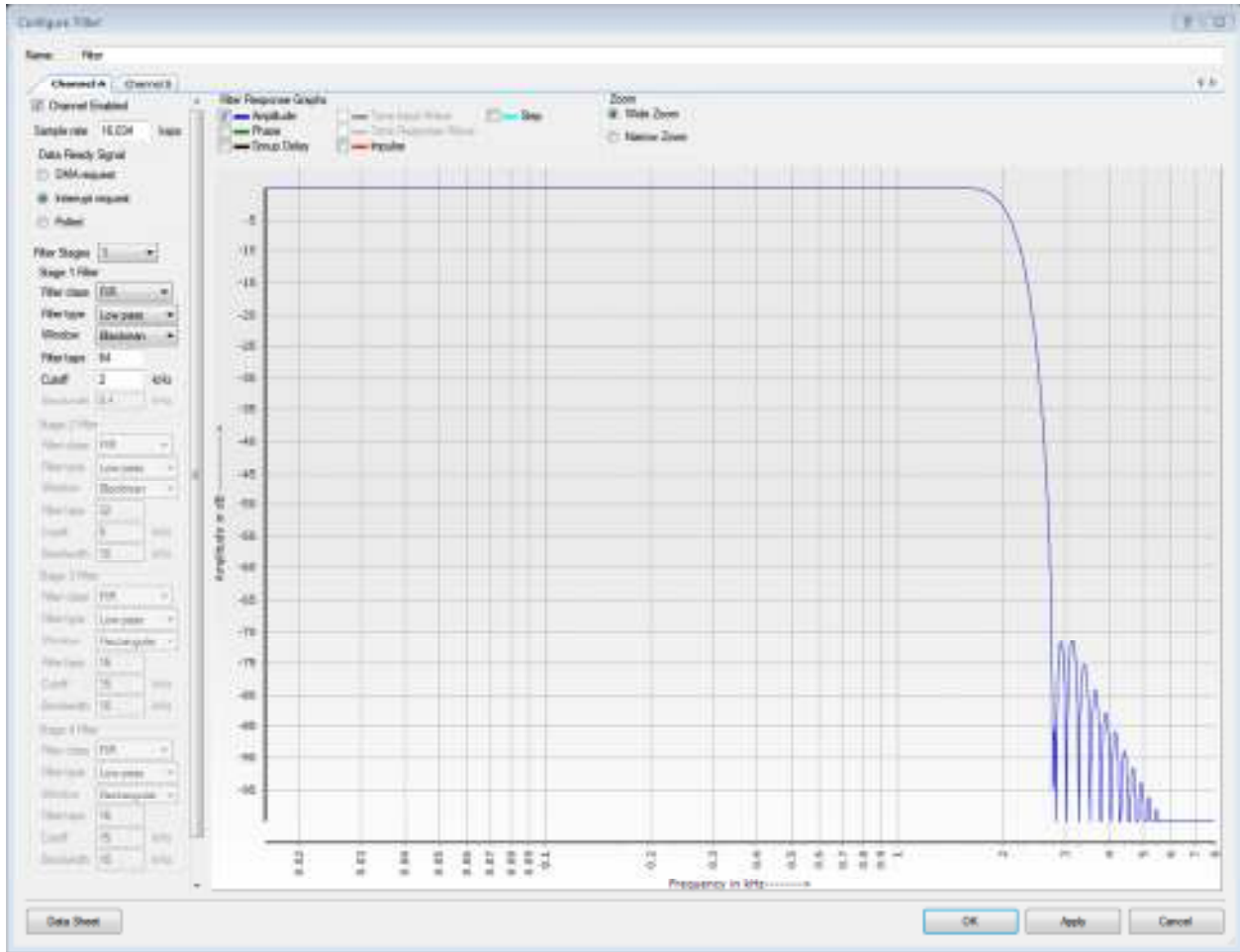


Figure 5: 2 KHz Audio digital low-pass filter response.

The output of the low-pass filter is fed into one of the PSoC's 8 bit digital to analog converters (DAC) that converts the data stream back into an analog signal. This signal is buffered with a unity gain op amp, U3, and passed to the output connector.

**Performance:**

The +5 volt power to the receiver is supplied by the host USB device, and is typically 55 to 60 mA.

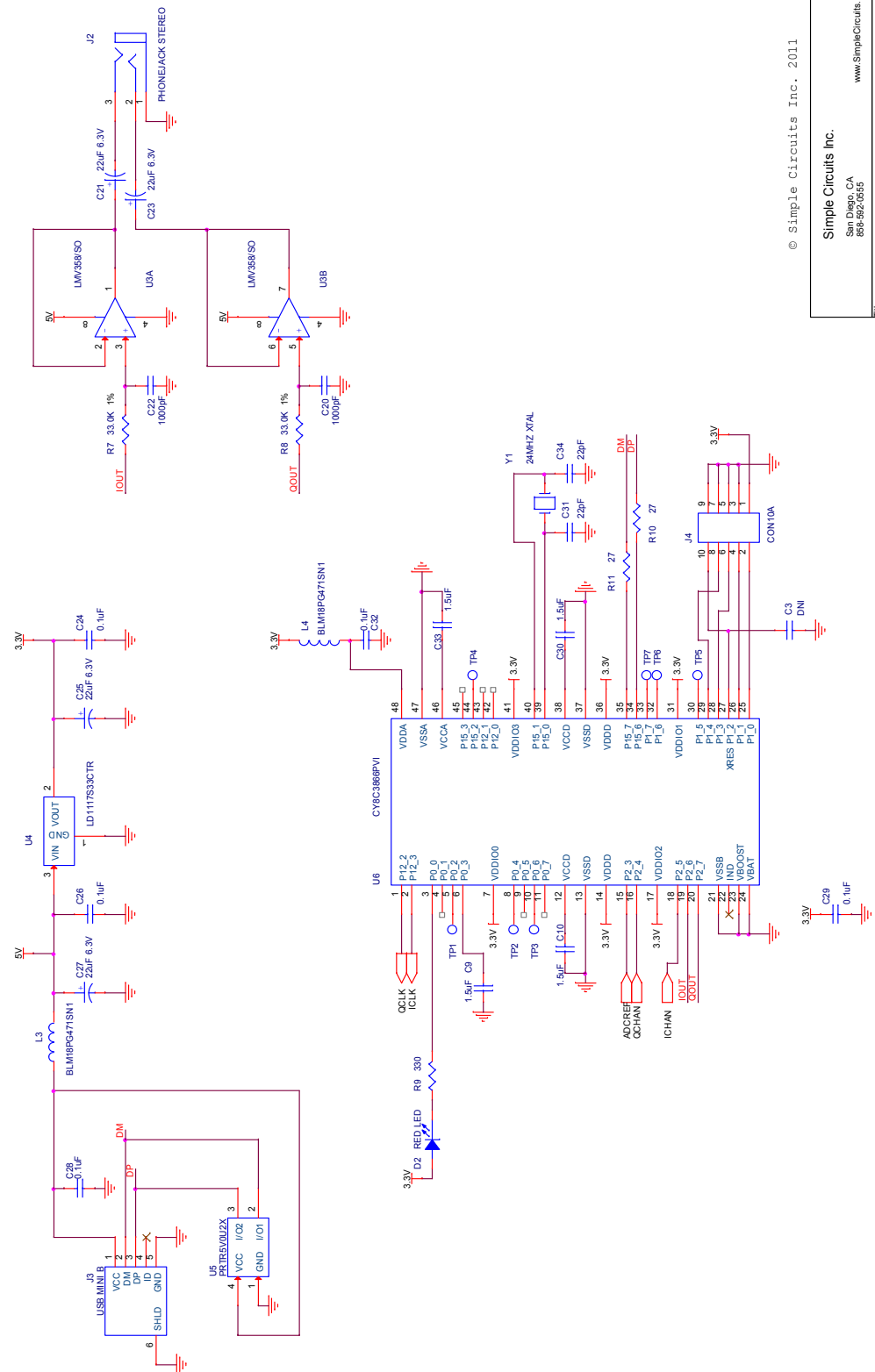
The frequency range of operation is controlled by the firmware. The current firmware limits the tuning to 3.500 MHz to 18.168 MHz. Higher frequencies are beyond the frequency range of the PSoC internal PLL circuit. Lower frequencies, such as the amateur 160 meter band, were overloaded from AM broadcast stations.

The minimum discernible signal (MDS) is approximately -117 dBm.

**Enclosure Modifications:**

To keep the cost of the receiver as low as possible, the unit is not in any enclosure. However, the board dimensions were specifically designed to fit in a Hammond Manufacturing model 1455B802 enclosure. The BNC connector must be removed and replaced with a through-chassis BNC connector.

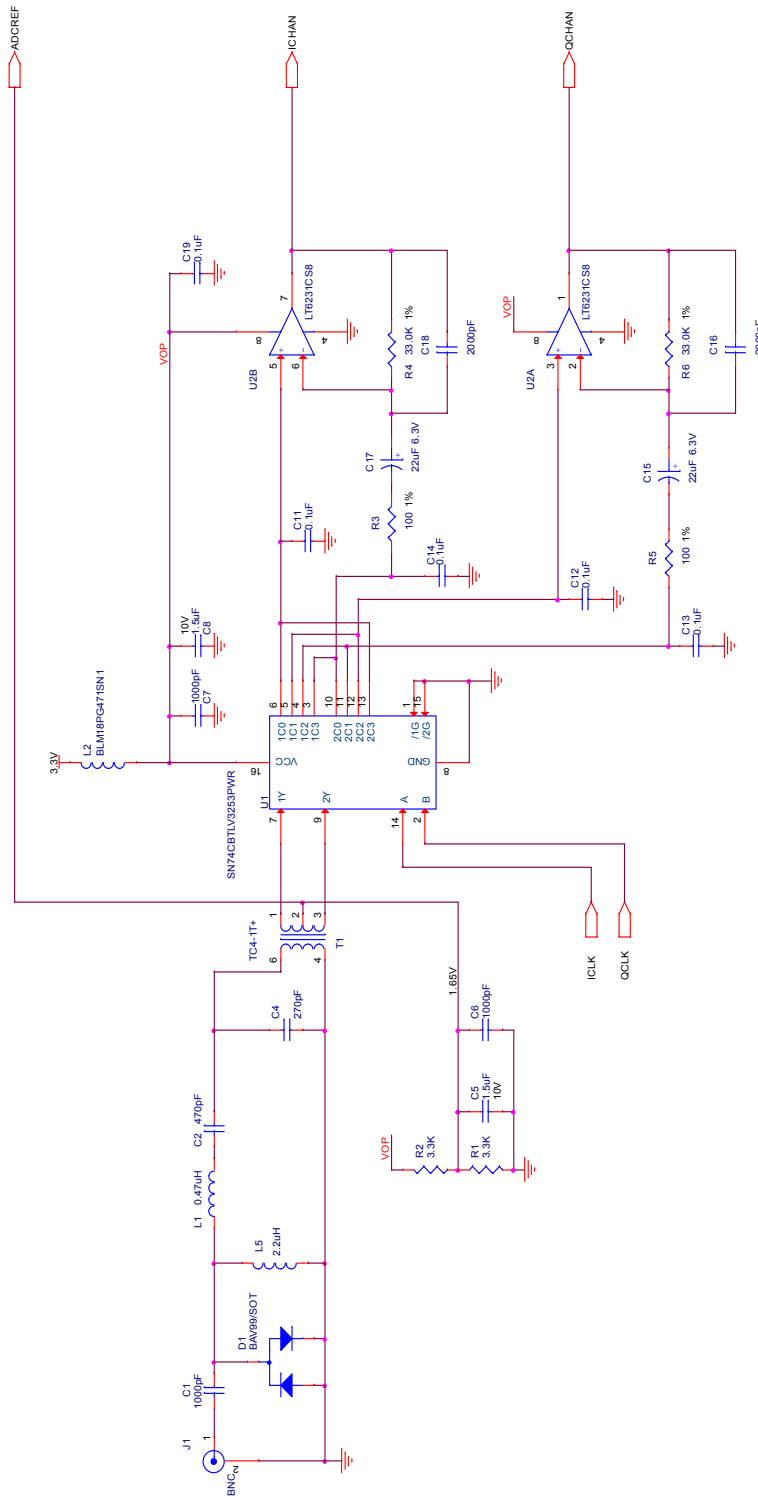




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Simple Circuits Inc.  
San Diego, CA  
858-592-0555

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